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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/757,491	01/11/2001	Haruo Tanaka	P107400-00021	8241

7590 07/26/2005

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EXAMINER
NGUYEN, JENNIFER T

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/757,491	TANAKA ET AL.	
	Examiner	Art Unit	
	Jennifer T. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2001*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,6,9 and 11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,6,9 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to amendment filed on 08/09/2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (Patent No. US 5,349,366) in view of Dawson et al. (Patent No. US 6,229,506).

Regarding claim 11, referring to Fig. 1A, Yamazaki teaches a display device comprising:

a display element (LC);

A MOS transistor (Tr2), a source and drain of said MOS transistor being connected to said display element an a driving line (Vlc);

a ferroelectric capacitor (FE) connected between a gate of said MOS transistor and a control line (Vd);

wherein the control data is written to said ferroelectric capacitor (FE) by using said control line (Vd) and said write line (Vlc) (col. 10, lines 21-38).

Yamazaki differs from claim 11 in that he does not specifically teach a capacitor connected between a gate and a write line. However, Dawson teaches a capacitor (450) connected between a gate (G of P1) and a write line (420) (Fig. 4, col. 5, lines 38-50). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention

was made to incorporate the capacitor as taught by Dawson in the system of Yamazaki in order to eliminate the back gate control and the cell can be high integrated.

Regarding claim 12, Yamazaki teaches a selective transistor (Tr1) is connected between said ferroelectric capacitor (FE) and said control line (Vd), and a gate of said selective transistor (Tr1) is connected to a selective line (Vg) (Fig. 1A).

Regarding claim 13, the combination of Yamazaki and Dawson teaches the display element is formed by an organic EL element (470) (Fig. 4 of Dawson).

4. Claims 3, 6, 9, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (Patent No. US 5,349,366) in view of Dawson et al. (Patent No. US 6,229,506) and further in view of Black et al. (Patent No. US 6,069,381).

Regarding claim 6, the combination of Yamazaki and Dawson teaches all limitations except the transistor is an MFMIS structure transistor which has a first metal layer, a ferroelectric layer, a second metal layer for gate electrode and an insulator layer provided on a semiconductor layer, a source and drain of said MFMIS structure transistor. However, referring to Fig. 7, Black teaches an MFMIS structure transistor which has a first metal layer (5), a ferroelectric layer (2), a second metal layer (7) for gate electrode and an insulator layer provided on a semiconductor layer (8), a source and drain (9) of said MFMIS structure transistor (col. 4, lines 46-67, col. 6, lines 1-13). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the MFMIS structure transistor as taught by Black in the system of the combination of Yamazaki and Black in order to provide a device which offers significant advantages for operation at low voltages and at high speed.

Regarding claim 3, Yamazaki teaches a selective transistor (Tr1) is connected between said nonvolatile data holding section (FE) and said control line (Vd), and a gate of said selective transistor is connected to a selective line (Vg) (Fig. 1A).

Regarding claims 9 and 15, the combination of Yamazaki, Dawson, and Black teaches the display element is formed by an organic EL element (470) (Fig. 4 of Dawson).

5. Claim 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (Patent No. US 5,349,366) in view of Black et al. (Patent No. US 6,069,381) and further in view of Hidaka et al. (Patent No. US 6,521,927).

Regarding claim 14, the combination of Yamazaki and Black teaches all the limitations except the nonvolatile data holding section is constituted by an element utilizing a single electron memory. However, Hidaka teaches the nonvolatile capacitor utilizing a single electron memory (DRAM) (col. 1, lines 18-24). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the nonvolatile data holding section as taught by Hidaka in the system of the combination of Yamazaki and Black in order to reduce power consumption.

6. Applicant's arguments with respect to claims 3, 6, 9, and 11-15 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer T. Nguyen whose telephone number is 571-272-7696. The examiner can normally be reached on Mon-Fri: 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick N. Edouard can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer Nguyen
7/19/05

REGINA LIANG
PRIMARY EXAMINER